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Docket Number FIS920020139US1	Applicant Number 107538905
Applicant(s) H. Bernhard Pogge et al.	not yet assigned
Filing Date herewith	Group Art Unit not yet assigned

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

/DG/		J.-Q. Lu et al., "Fabrication of via-chain test structures for 3D IC technology using dielectric glue bonding on 200 mm wafers," Materials Research Society ULSI XVII Conference Proceedings 151 (2002)
/DG/		P. Ramm et al., "Interchip via technology by using copper for vertical system integration," Materials Research Society Advanced Metallization Conference 159 (2002)

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